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LOW THRESHOLD VOLTAGE TRANSISTOR DISPLACEMENT IN A SEMICONDUCTOR DEVICE

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BACKGROUND

Field of the Invention

[1001] The present invention relates generally to techniques for designing and optimizing semiconductor devices and, in particular, to automated techniques for substituting low threshold voltage transistor, gate, or cell instances in a semiconductor design.

Description of the Related Art

[1002] Integrated circuit designers may replace standard threshold voltage (V_t) transistors with low V_t transistors in critical circuit paths to increase clock speeds of high-speed circuits while meeting semiconductor device process limitations. In general, low V_t transistors have a reduced intrinsic delay as compared to corresponding standard V_t cells. As a result, use of a low V_t cell instance in substitution for a cell instance that contributes to a maximum time violation in a timing path may allow an integrated circuit design to operate at a higher frequency. However, under some circumstances, low V_t cells may exhibit increased intrinsic delays as compared to standard V_t cells. For example, devices manufactured using one process technology may exhibit an increase in the intrinsic delay of a low V_t cell as compared to a standard V_t counterpart for falling edge transitions at the inputs of higher fan-in cells. Accordingly, there is a need for a technique that identifies these low V_t cells that reduce performance as compared to standard V_t cells, and selectively replaces these low V_t cells with standard V_t cells to improve circuit performance.

SUMMARY

[1003] A mechanism has been developed by which the performance of an integrated circuit design can be improved by selectively replacing low V_t transistors with standard V_t transistors. In some embodiments of the invention, the selection of gates for replacement is based on a multi-path timing analysis. This timing analysis may include information on path cycle time, device type, and input slew rates for each device in the path. The input slew rates may include information on falling edge input transitions, in addition to rising edge transitions. This timing analysis may be performed for every path that includes a low V_t variant of a gate instance.

[1004] In some embodiments of the invention, if a low V_t variant of a gate instance increases a path cycle time as compared to a standard V_t counterpart, the maximum of the path cycle times for all paths that include the low V_t variant is calculated. A maximum of the path cycle times for these paths with a standard V_t variant substituted for the low V_t variant is also calculated. In some embodiments, the selection mechanism compares these two maximum cycle times. If the maximum path cycle time for the path including the low V_t variant is greater than the maximum path cycle time for the path including the standard V_t variant, then that low V_t variant is substituted with a standard V_t variant. As a result, integrated circuit designs prepared in accordance with the present invention may exhibit substantial cycle time improvements.

BRIEF DESCRIPTION OF THE DRAWINGS

[1005] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[1006] **FIG. 1** depicts information and control flows for a technique for processing a design for a semiconductor device in accordance with some embodiments of the present invention.

[1007] **FIG. 2** depicts information and control flows for a technique for processing design files.

[1008] The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION OF THE INVENTION

[1009] The developed substitution techniques are, in general, applicable at a variety of levels of design hierarchy, such as at the individual device, transistor, or FET gate level, at the logic gate or standard cell level, or at larger circuit block levels. In each case, a standard V_t instance may be selectively substituted for a low V_t instance. The low V_t variants may have been replacements for standard V_t gate instances in critical circuit paths. For example, one suitable mechanism for low V_t transistor substitution in an integrated circuit is described in detail in commonly-owned, co-pending United States Patent Application No.: 10/098,756, entitled "LOW V_t TRANSISTOR SUBSTITUTION IN A SEMICONDUCTOR DEVICE," the entirety of which is incorporated herein by reference. Persons of ordinary skill in the art will appreciate that a low V_t logic gate instance or circuit block may, in general, include one or more low V_t devices or transistors. Selective substitution may be made at any level of design hierarchy appropriate to a particular integrated circuit design and/or design environment. For purposes of clarity, much of the description that follows is expressed in the context of instances of standard cells that implement logic gates. Accordingly, in some realizations, particular gate instances and low V_t gate instances may correspond to instances of standard cells and timing analyses, and substitutions will be performed at levels of hierarchy corresponding to such instances and networks thereof. However, more generally, the terminology "gate instance" and "low V_t gate instance" will be understood to include instances of integrated circuit structures and features ranging from individual instances of devices, transistors or gates, to individual instances of logic gates or flops, to instances of circuit blocks. Of course, not all transistors or other devices of a low V_t logic gate or circuit block need be low V_t transistors or devices and suitable designs, including standard cell designs, for low V_t logic gates or circuit blocks will be understood by persons of ordinary skill in the art.

[1010] In view of the foregoing, and without limitation, aspects of an exemplary exploitation of the developed techniques are now described in the context of networks of standard cell logic gate instances, timing analysis thereof, and substitutions of low

V_t variants with standard V_t variants of the standard cells. Based on the description herein, persons of ordinary skill in the art will appreciate suitable exploitations for gate instances at a variety of levels of design hierarchy.

[1011] Referring to FIG. 1, a method of processing a design for a semiconductor device is illustrated. The method includes evaluating circuit timing paths in a design file including the low threshold voltage (V_t) variants of gate instances (102). Low V_t variants are selected for replacement (104). Next, the design is modified to include standard V_t variants substituted for the selected low V_t variants (106). This may be achieved by swapping information corresponding to the low V_t physical files, low V_t schematic representations, and low V_t timing files with those for the respective standard V_t cells. In a particular implementation, two substantially co-extensive cell libraries may be provided. For example, a standard V_t library may be provided that includes standard V_t type transistors, circuit and gate configurations implementing cells of the library, while a low V_t library includes low V_t type transistors and circuit and gate configurations implementing corresponding cells. In such an implementation, swapping a particular cell instance from low V_t to standard V_t simply involves substituting information for a corresponding cell from a different library. After the selected cells of the design have been substituted from low V_t to standard V_t cells, design verification tests, such as noise tests, minimum timing tests, and physical verification tests, may be re-executed (108) to verify the new design that includes the substituted low V_t cells. The design file may then be used to fabricate a semiconductor chip (110) according to any procedure for manufacturing a semiconductor chip known in the art.

[1012] A method for selecting low V_t variants for replacement is illustrated in FIG. 2. This method generates a maximum timing report for a design including only standard V_t devices and a maximum timing report for the same design including at least one low V_t device. These timing reports may include information about path cycle times, device delays, device type, and slew rate for rising and falling edge transitions of the signal at each node. Each instance of a low V_t device may reside in multiple paths. The method compares the gate delays of the low V_t device and its corresponding standard V_t counterpart for a path including the low V_t device (202). In one realization, if the cycle time for the path including the low V_t device is shorter

than the cycle time for the path including only standard V_t devices, then that low V_t device produces a "speedup." If the cycle time for the path including the low V_t device is longer than the cycle time for the path including only standard V_t devices, then that low V_t device produces a "slowdown," or timing penalty.

[1013] For each path including a low V_t device that produces a slowdown, the method then computes a path cycle time for every path including that low V_t device (204) and a path cycle time for those same paths but with a standard V_t device substituted for the low V_t device (206). For each low V_t device that produces a slowdown for any path, the method computes the maximum of the path cycle times for each path including the low V_t device (208) and the maximum of the path cycle times for that path without the low V_t device (210). If the maximum of the path cycle times for each path including the low V_t device is less than or equal to the maximum of the path cycle times for that path without the low V_t device, then that low V_t device will not be replaced by a standard V_t device (212). If the maximum of the path cycle times for each path including the low V_t device exceeds the maximum of the path cycle times for that path without the low V_t device by a threshold penalty, then that low V_t device is selected for replacement with a standard V_t device (214). In one embodiment, the threshold penalty is design-dependent and equals one picosecond for an exemplary 130nm process technology. The method does not replace a low V_t device with a standard V_t device when the maximum of the path cycle times for each path including the low V_t device is equal to the maximum of the path cycle times for that path without the low V_t device because a device that receives its inputs from a low V_t device may have improved performance than a device that receives its inputs from a standard V_t device.

[1014] Examples for steps 204-214 of the invention are illustrated for an exemplary circuit design in Tables 1 and 2. A low V_t device is identified in steps 202-206 that produces a slowdown for at least one design path including this device. The device occurs in three design paths. For each of these paths, the path cycle time is computed for the path including the low V_t device, and for the path without the low V_t device speedup or slowdown. The maximum path cycle time with the low V_t device is 300 ps. The maximum path cycle time for the path without the low V_t device speedup or slowdown is 296 ps. Since the maximum path cycle time for the

path without the low V_t device is less than the maximum path cycle time for the path including the low V_t device, the method selects this low V_t device for replacement by a standard V_t device.

Path	Timing penalty	Effect of LV_t on path cycle time	Path cycle time with LV_t device	Path cycle time without LV_t device penalty
1	-5	Slowdown	295 ps	290 ps
2	+11	Speedup	285 ps	296 ps
3	-7	Slowdown	300 ps	293 ps

Table 1: Example of method for a low V_t device that occurs in three paths

[1015] However, if the slowdown in path 3 for this design is -2, as displayed in Table 2, the low V_t device will not be selected for replacement. The maximum path cycle time with the low V_t device is now 295 ps, which is less than the maximum path cycle time for the path without the low V_t device speedup or slowdown of 296 ps. Although the low V_t device produces a slowdown in two of three paths, this device is not replaced with a standard V_t device because it provides an improvement in the maximum path cycle times.

Path	Timing penalty	Effect of LV_t on path cycle time	Path cycle time with LV_t device	Path cycle time without LV_t device
1	-5	Slowdown	295 ps	290 ps
2	+11	Speedup	285 ps	296 ps
3	-2	Slowdown	295 ps	293 ps

Table 2: Example of method for a low V_t device that occurs in three paths

[1016] A method consistent with the previous discussion may be embodied in an automated computer software semiconductor design tool for processing design files, which may be executed on a programmable computer. In one exemplary embodiment, software implemented as PERL scripts selects low V_t variants for replacement by processing design files generated by Millennium Delay Calculator, available from Celestry Design Technologies, Inc., and PEARL Static Timing

Analyzer, available from Cadence Design Systems, Inc. In addition, design tools that support VERILOG or other hardware description languages may be employed. Persons of ordinary skill in the art will recognize a variety of design tools and languages appropriate for implementing the teaching described herein. Other variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.